latching the first data bit i[redacted]e master latch and loading the firs[redacted]ta bit into the slave latch comprise generating the clock signal having a second clock state.

Cont A'

REMARKS

Claims 1 - 37 are pending in this broadening reissue application.

The Applicant has amended the drawings to correct a minor error as discussed in the enclosed Request for Drawing Change.

The Applicant has amended the specification to correct minor errors.

The Applicant has added new method claims 18 - 37, which the Applicant believes broaden the scope of protection to his invention.

The Applicant has added no new matter to the reissue application.

In light of the foregoing, original claims 1 – 17 as issued and new claims 18 – 37 are in condition for full allowance, and that action is respectfully requested.

If the Examiner believes that a phone interview would be helpful, he is respectfully requested to contact the Applicant's attorney, Bryan Santarelli, at (425) 455-5575.

DATED this 15th day of June, 2000.

Respectfully submitted,

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Enclosures